REMARKS

I. Introduction

Claims 1-14 are pending in this application, of which claims 1 and 10 are independent. The Examiner withdrew the previous rejection of the claims, but cited a new reference, Yamasaki, to reject the claims in combination with Yuzurihara of record.

II. The Present Invention

Before discussion of the rejection of claims 1-14, a brief explanation of the present invention is provided.

The present invention relates to a solid-state imaging apparatus that achieves less leakage current, high image quality, and low noise during the driving operation, and manufacturing method for the same.

To achieve the above object, the solid-state imaging apparatus includes an imaging region and a driving circuit region both formed on one semiconductor substrate. The image region includes an active-type unit pixel in which a photodiode unit generates signal charge by photoelectric conversion and an amplification unit amplifies the signal charge. The drive circuit region includes, for example, at least a vertical shift resistor and a horizontal shift resistor, and drives the photodiode unit and the amplification unit. In the solid-state imaging apparatus according to claim 1, the imaging regions and the drive circuit region include one or more transistors, respectively, and all the transistors in the imaging region and the drive circuit region have the same channel polarity.

The solid-state imaging device having the above-described configuration is manufactured by using the conventional CMOS processing technology. The number of processes required for

forming all the transistors in both regions is only approximately a half the number of processes required for manufacturing the conventional solid-state imaging apparatus with use of the CMOS processing technology. This means that the imaging region suffers less damage during the process for forming the transistors.

Therefore, the solid-state imaging apparatus according to claim 1 achieves less noise in the amplification unit and less leakage current in the photodiode unit, resulting in less deterioration of the image quality caused by the noise and the leakage current.

Regarding the manufacturing method, all the transistors formed in the image region and the drive circuit region have the same channel polarity. Accordingly, it is possible to manufacture a solid-state imaging apparatus that suffers less noise in the amplification unit and less leakage current in the photodiode unit, and achieves high image quality.

III. The Rejection of Claims 1-5, 10, and 11

Claims 1-5, 10, and 11 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yuzurihara in view of Yamasaki. In the statement of the rejection of independent claim 1, the Examiner admitted that Figs. 1 and 11 of Yuzurihara do not disclose that all the transistors in the imaging region and the drive circuit region have the same channel polarity. However, the Examiner asserted that Yamasaki discloses the missing feature of Yuzurihara, and concluded that it would have been obvious to form the solid-state imaging apparatus of Yuzurihara with the transistors of Yamasaki in order to decrease the number of process required for forming all the transistors, decrease the leakage current, decrease the noise during driving operation, and increase the image quality. Applicant respectfully traverses this rejection.

Applicant submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §103 for lack of the requisite factual basis. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). In imposing a rejection under 35 U.S.C. §103, the Examiner is required to make a "thorough and searching" factual inquiry and, based upon such a factual inquiry, explain why one having ordinary skill in the art would have been realistically impelled to modify particular prior art to arrive at the claimed invention. *In re Lee*, 277 F.3d 1338, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002). Such motivation must be based upon "clear and particular" showings of combinability in the prior art -- not in the application disclosure. *Panduit Corp. v. Dennison Mfg. Co.*, 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985).

Applicant submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention for lack of the requisite factual basis. Specifically, Yuzurihara and Yamasaki, either individually or in combination, do not teach, at a minimum, "a solid-state imaging apparatus that includes an imaging region and a drive circuit region both formed on one semiconductor substrate, ... wherein all the transistors in the imaging region and the drive circuit region have a same channel polarity," recited in independent claim 1 (emphasis added).

Yuzurihara discloses a solid-state imaging apparatus in an imaging region of which n-type MOS transistors are formed, and in a peripheral region of which n-type MOS transistors and p-type MOS transistors produced by a CMOS processing technology are formed (paragraph [0061]).

In the solid-state imaging apparatus disclosed in Yuzurihara, n-channel MOS transistors are formed in the imaging region, and n-channel MOS transistors and p-channel MOS transistors are formed in the driving circuit region. In contrast, claim 1 recites that all the transistors in the imaging region and the drive circuit region have the same channel polarity. It is, therefore, apparent that Yuzurihara's apparatus is different from what is claimed, as admitted by the Examiner.

Yamasaki discloses a photoelectric conversion apparatus for focus detection. Fig. 3 of Yamasaki discloses a structure including a barrier gate in a monitor unit (monitor means), a photo diode in the monitor unit, a photodiode array in a pixel element (photoelectric transducer element), a barrier gate, a storage gate and a transfer gate in the pixel element. The CCD-type photoelectric conversion apparatus for focus detection disclosed in Yamasaki includes an amplifier circuit comprising transistors Q1 to Q5 and outputs the signal charges of the monitor unit, and an amplifier circuit comprising transistors Q6 to Q10 and a photodiode D1 and outputs the signal charges of the pixel element. According to Yamasaki, all of the transistors Q1 to Q10 are n-type MOS transistors.

However, in the photoelectric conversion apparatus for focus detection according to Yamasaki, the amplifier circuit comprising transistors Q1 to Q5 and the amplifier circuit comprising transistors Q6 to Q10 are both circuits for amplifying signal charge of photodiodes, and not equivalent to the drive circuit for driving each photodiode unit included in the pixel. In contrast, claim 1 address transistors not only in the imaging region but also in the drive circuit region for driving the photodiode unit and the amplification unit. Accordingly, Yamasaki does not teach, "all the transistors in the imaging region and the drive circuit region have a same channel polarity," recited in claim 1.

Moreover, in the photoelectric conversion apparatus for focus detection according to Yamasaki (Fig. 2), the CCD image sensor and the CCD driver are provided as two separate chips. Yamasaki relates to a CCD image sensor, and the imaging region and the driving circuit region are formed as separate chips. In contrast, claim 1 recites "an imaging region and a driving circuit region both formed on one semiconductor substrate." Therefore, it is apparent that Yamasaki is different from the claimed invention because Yamasaki does not teach "a solid-state imaging apparatus that includes an imaging region and a drive circuit region both formed on one semiconductor substrate, ... wherein all the transistors in the imaging region and the drive circuit region have a same channel polarity," recited in claim 1 (emphasis added).

Accordingly, Yuzurihara and Yamasaki, either individually or in combination, do not teach, at a minimum, a solid-state imaging apparatus including all the limitations recited in independent claim 1.

Applicant further submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention for lack of the requisite realistic motivation to combine the cited prior art. The Examiner's asserted motivation is to decrease the number of processes required for forming all the transistors, decrease the leakage current, decrease the noise during driving operation, and increase the image quality (paragraph bridging pages 3 and 4 of the Office Action).

In response, Applicant submits that the Examiner has not discharged his burden of making a "thorough and searching" factual inquiry and, based upon such a factual inquiry, explain why one having ordinary skill in the art would have been realistically impelled to modify particular prior art to arrive at the claimed invention. *In re Lee*, *supra*. In other words, the Examiner did not indicate where the prior art references teach process reduction, leakage current

and noise decrease, and image quality increase that can be relied upon as the basis for the necessary motivation. Facts are required. *In re Lee, supra.*

Moreover, the Examiner is not allowed to rely on the application disclosure to show that there is motivation to modify the device of Yuzurihara to arrive at the claimed invention. *Panduit Corp., supra.* Yuzurihara and Yamasaki do not disclose or suggest the problems associated with the prior art devices or the need for process reduction, leakage current and noise decrease, or image quality increase (see, e.g., Yuzurihara, paragraph [0012]; Yamasaki, column 2, lines 12-21). However, such teaching can be found in the specification of the present application. The present application describes as follows:

> However, the conventional MOS type imaging apparatuses manufactured based on such a CMOS processing technology might suffer, in the imaging region, leakage current in the photodiode unit and characteristic deterioration in the amplification circuit during the driving operation, which become causes of a noise. When a noise is caused in the imaging region, it is amplified and output with the signal charge, resulting in deterioration of the image quality.

Page 5, lines 23 to page 6, line 4. Applicant respectfully requires the Examiner to show evidential support for the asserted motivation.

Based upon the foregoing, Applicant submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention in independent claim 1 for lack of the requisite factual basis and want of the requisite realistic motivation. The above discussion is applicable to a manufacturing method in independent claim 10. Dependent claims 2-5 and 11 are also patentably distinguishable over Yuzurihara and Yamasaki at least because these claims include all the limitations recited in independent claims 1 and 10, respectively. Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 1-5, 10, and 11 under 35 U.S.C. §103, and favorable consideration thereof.

III. The Rejection of Claims 6-9 and 12-14

Claims 6-8 and 12-14 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yuzurihara in view of Yamasaki and further in view of Momose et al.; and claim 9 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Yuzurihara in view of Yamasaki and further in view of Shinohara et al.

Each of the above rejections under 35 U.S.C. § 103 is traversed. Specifically each of claims 6-8 and 12-14 depend from independent claims 1 and 10, Applicant incorporates herein the arguments previously advanced in traversing the imposed rejection of claims 1 and 10 under 35 U.S.C. §103. Momose et al. and Shinohara et al. do not cure the previously argued deficiencies of the applied combination of Yuzurihara and Yamasaki.

Applicants, therefore, submit that the imposed rejection of claims 6-9 and 12-14 under 35 U.S.C. §103 is not factually or legally viable and, hence, respectfully solicit withdrawal thereof.

IV. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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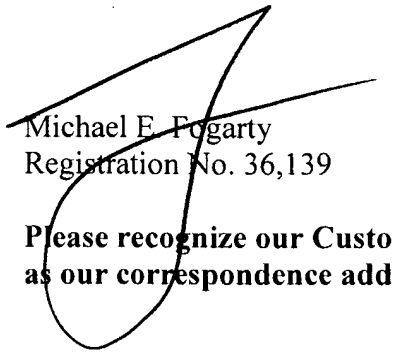

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